extending through the supporting member and electrically coupled in series with the second capacitor plate which is the conductive glue. This construction has numerous advantages. See page 5, lines 15-27, through page 6, lines 1-2, of the specification.

Claims 1-4, 7, 9-10, 17 and 20-21 stand rejected under 35 U.S.C. §102 as being anticipated by United States Patent 4,736,521 (Dohya). This ground of rejection is traversed with respect to newly submitted claims 22-49 for the following reasons.

The Examiner correctly recognizes that Dohya does not disclose a first capacitor plate which comprises a layer of conductive glue. This is stated in Section 9 of the Office Action regarding the rejection of claims 6, 8 and 19 as being unpatentable over Dohya in view of EP 630 176.

Neither EP 630,176 or GB 2118371 discloses a layer of conductive glue used as part of a ground plane for a semiconductor chip. With respect to GB 2118371, conductive bumps 27, 28a, 28b, 29a and 29b are disclosed but these bumps do not constitute or would be considered by a person of ordinary skill in the art to be conductive glue or the equivalent of a conductive glue. The Examiner is referred to the Abstract of the Disclosure and further to page 2, column 1, lines 16-32, for a description of the bumps which are not described as glue. This is contrary to the Examiner's statement of the rejection in Section 6 of the Office Action wherein the Examiner states that GB 2118371 disclose..."wherein the chip (12) is adhered to the supporting member (14) by means of a conductive glue (27, 28a, 28b, 29a, 29b are solder) and the

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conductive glue is in electrical contact with the metal covered area". A person of ordinary skill in the art would not consider solder to be a conductive glue with soldering having disadvantageous properties of requiring heat to secure bonding.

EP 0630176 has been erroneously construed by the Examiner to disclose conductive glue. The Assignee's European representative states that the description in Dobers is to "thermally conductive glue" and not electrically conductive glue. Accordingly, Dobers et al cannot be relied upon for teaching to utilize electrically conductive glue and is concerned with the removal of heat from an electrical assembly. A copy of an English language Abstract from the EPO internet site is submitted herewith for making of record by the Examiner in the attached Form 1149.

Newly submitted claim 22 recites, *inter alia*, a ground plane for a semiconductor chip...wherein the second capacitor plate comprises a layer of conductive glue". It is submitted that a person of ordinary skill in the art would not be led to modify the teachings of Dohya in view of either GB 2118371 or EP 0630176 in view of neither a teaching of conductive glue. The solder connections of GB 2118371, as stated above, are not properly considered by a person skilled in the art to read upon the claimed layer of conductive glue. Moreover, a person of ordinary skill in the art would not be led to modify the teachings of the use of solder of GB 2118371to utilize a conductive glue as set forth in claims 22-47.

Claim 23 further defines the ground plane as having a resonant frequency provided by the capacitance of the first capacitor plate and the second capacitor

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plate and the inductance provided by the at least one first conducting member approximately equal to an intended working frequency of the chip. This subject matter is not disclosed in Dohya, GB 2118371 and EP 0630176.

Dependent claims 24-47 define further aspects of the invention which are neither anticipated nor rendered obvious by the prior art of record.

Claim 48 defines a method for providing a ground plane for a semiconductor chip mounted on a supporting member in a chip package comprising providing a metal cover area on the surface of the supporting member, providing vias electrically connected to the metal covered area and extending therefrom through the supporting member to the opposite side thereof, connecting in parallel at least two of the vias, and using a conductive glue between the chip and the metal covered areas to attach the metal covered area to the chip. As has been stated above, the solder of GB 2118371 does not read upon and cannot be construed to motivate a person of ordinary skill in the art to use the claimed conductive glue in the recited method of providing a ground plane.

Claim 49 defines a semiconductor chip passage comprising a semiconductor chip and a supporting member, the supporting member comprising at least one metal covered area and at least one electrically conductive via extending from the metal covered area through the supporting member, wherein the chip is adhered to the supporting member by means of a conductive glue and the conductive glue is in electrical contact with the metal covered area. Claim 49 is patentable for the same reasons set forth above with regard to claim 48. None

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of the prior art of record, including EP 630,176 or GB 2118371, teaches the use of conductive glue and would not motivate a person of ordinary skill in the art to utilize conductive glue as set forth in the semiconductor chip passage of claim 49.

It should be noted by the Examiner that GB 2118371 has been cited as an "X" category document in a corresponding Great Britain Search Report. However, the deficiencies of GB 2118371 have been pointed out above.

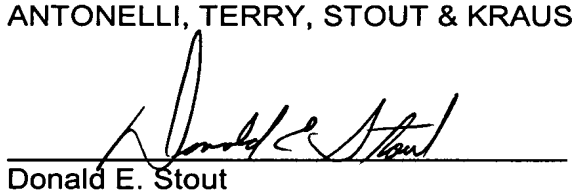
Concurrently filed herewith is a Request for Authorization to Amend the Drawings to add reference numerals 20 and 22 as described in the amended specification.

In view of the foregoing amendments and remarks, it is submitted that each of the claims in the application is in condition for allowance.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (612.38837X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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